IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of

KIMURA et al.

Serial No. 10/668,166

Filed: September 24, 2003

Title: SEMICONDUCTOR DEVICE AND CHIP-STACK SEMICONDUCTOR DEVICE

Atty Dkt. JAR-1035-473
C# M#
Confirmation No. 4031
TC/A.U.: 2811
Examiner: ARENA, Andrew O.
Date: July 2, 2008

1st AFS

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

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Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting applicant's claim(s). $510.00 (1401)/$255.00 (2401) $

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By Atty: Joseph A. Rhoa, Reg. No. 37,515

Signature: by Michael J. Keenan #32,106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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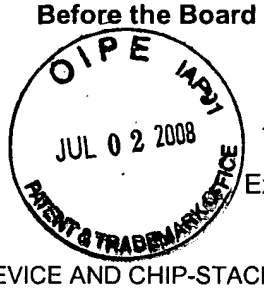
In re Patent Application of



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* *

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APPEAL BRIEF

Sir:

Appellant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner.

07/03/2008 JADD01 00000113 10668166
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TABLE OF CONTENTS

(I) REAL PARTY IN INTEREST

The real party in interest is Sharp Kabushiki Kaisha, a corporation of the country of Japan.

(II) RELATED APPEALS AND INTERFERENCES

The appellant, the undersigned, and the assignee are not aware of any related appeals, interferences, or judicial proceedings (past or present), which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

(III) STATUS OF CLAIMS

Claims 1-2, 4-5, 7-9, 11-13, 15-17, and 19-20 are pending and have been rejected. Claims 3, 6, 10, and 14 have been cancelled. No claims have been substantively allowed.

(IV) STATUS OF AMENDMENTS

No amendments have been filed since the date of the Final Rejection.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

This section is for purposes of example only and is without limitation on the scope of the claims.

Claim 1 relates to a semiconductor device (e.g., 10 in Fig. 1(a); p. 11, lines 19-20). A plurality of spaced apart through electrodes (e.g., 8 in Fig. 1(a); p. 11, lines 20-23) with equal cross-sectional areas (e.g., p. 11, line 24 to p. 12, line 3) in a semiconductor chip (e.g., 1 in Figs. 1(a) and 1(b)) are provided, which through electrodes electrically link a front surface of the chip to a back surface of the chip (e.g., see Fig. 2). At least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply (e.g., 8a in Fig. 1(a); p. 12, lines 4-18; p. 16, lines 7-18). At least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground (e.g., 8b in Fig. 1(a); p. 12, lines 4-18; p. 16, lines 7-18). A particular signal-routing through electrode is formed of only one of the plurality of through electrodes (e.g., 8c in Fig. 1(a); p. 12, lines 4-18; p. 13, lines 2-6). At least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip (e.g., 19 in Fig. 3; p. 17, lines 5-12).

Claim 5 relates to a chip-stack semiconductor device (e.g., 40 in Fig. 10; p. 24, line 25 to p. 25, line 3), comprising multiple stacked semiconductor chips (e.g., 1 in Fig. 10; p. 25, lines 4-9), each of the semiconductor chips including a semiconductor device

according to claim 1 (e.g., see above for an example mapping of the features of claim 1 to the specification; 1 in Fig. 10; p. 24, line 25 to p. 25, line 9).

Claim 7 relates to a chip-stack semiconductor device (e.g., 40 in Fig. 10; p. 24, line 25 to p. 25, line 9). A plurality of stacked semiconductor chips are provided (e.g., 1 in Fig. 10; p. 24, line 25 to p. 25, line 9). Each of the semiconductor chips includes a number of through electrodes (e.g., 18, 8b, and 8c in Fig. 10; p. 11, lines 20-23; p. 25, line 10 to page 26, line 3) with equal cross-sectional areas therein linking a front surface to a back surface thereof (e.g., see Fig. 10; p. 11, line 24 to p. 12, line 3). At least one of a first high-current through electrode connected to a power supply (e.g., 8a in Fig. 1(a); p. 12, lines 4-18; p. 16, lines 7-18) and a second high-current through electrode connected to ground (e.g., 8b in Fig. 10; p. 12, lines 4-18; p. 16, lines 7-18; p. 25, lines 18-24) is made up of at least two of the through electrodes which are electrically connected to one another, whereas a signal-routing electrode connecting a front a back surface of one of the semiconductor chips is made up of only one of the through electrodes (e.g., 8c in Fig. 10; p. 12, lines 4-18; p. 13, lines 2-6; p. 25, lines 10-17). At least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed so that said least one through electrode is not electrically connected to any electrode pad of the chip (e.g., 19 in Fig. 3; p. 17, lines 5-12; p. 28, lines 2-7).

Claim 8 relates to a chip-stack semiconductor device (e.g., 40 in Fig. 10; p. 24, line 25 to p. 25, line 9). Multiple stacked semiconductor chips are provided (e.g., 1 in Fig. 10; p. 24, line 25 to p. 25, line 9). Each of the semiconductor chips includes a

number of through electrodes (e.g., 18, 8b, and 8c in Fig. 10; p. 11, lines 20-23; p. 25, line 10 to page 26, line 3) with equal cross-sectional areas therein linking a front surface to a back surface thereof (e.g., see Fig. 10; p. 11, line 24 to p. 12, line 3). The number of the through electrodes is determined in accordance with a magnitude of an electric current to be conducted therethrough (e.g., p. 22, lines 13-25). Adjacent connected ones of the through electrodes which are connected to a either a ground terminal (e.g., 8b in Fig. 10; p. 12, lines 4-18; p. 16, lines 7-18; p. 25, lines 18-24) or a power supply terminal (e.g., 8a in Fig. 1(a); p. 12, lines 4-18; p. 16, lines 7-18) of that semiconductor chip are greater in number (e.g. p. 12, lines 15-18) than adjacent connected ones of the through electrodes which are connected to a particular signal terminal (e.g., 8c in Fig. 10; p. 12, lines 4-18; p. 13, lines 2-6; p. 25, lines 10-17) thereof. At least one of the through electrodes is a non-contact through electrode which is not electrically connected to any electrode pad of the chip in which it is formed (e.g., 19 in Fig. 3; p. 17, lines 5-12; p. 28, lines 2-7).

In addition to the features of claim 5, claim 9 recites a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2 (e.g., see Figs. 10 and 14; page 30, lines 5-10).

In addition to the features of claim 7, claim 11 recites a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2 (e.g., see Figs. 10 and 14; page 30, lines 5-10).

In addition to the features of claim 8, claim 12 recites a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2 (e.g., see Figs. 10 and 14; page 30, lines 5-10).

In addition to the features of claim 5, claim 13 recites as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for the first high-current through electrode and the second high-current through electrode (e.g., p. 30, line 23 to p. 32, line 3).

In addition to the features of claim 7, claim 15 recites the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for the first high-current through electrode and the second high-current through electrode (e.g., p. 30, line 23 to p. 32, line 3).

In addition to the features of claim 8, claim 16 recites as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for a first high-current through electrode and a second high-current through electrode (e.g., p. 30, line 23 to p. 32, line 3).

In addition to the features of claim 13, claim 17 recites numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (e.g., p. 30, line 23 to p. 32, line 3).

In addition to the features of claim 15, claim 19 recites numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (e.g., p. 30, line 23 to p. 32, line 3).

In addition to the features of claim 16, claim 20 recites numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (e.g., p. 30, line 23 to p. 32, line 3).

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-2, 4-5, 7-9, 11-13, 15-17, and 19-20 are unpatentable under 35 U.S.C. § 103(a) over Sumikawa (U.S. Patent No. 6,362,529) in view of Anderson (U.S. Patent No. 6,661,100).

(VII) ARGUMENT

Claims 1-2, 4-5, 7-9, 11-13, 15-17, and 19-20 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Sumikawa (U.S. Patent No. 6,362,529) in view of Anderson (U.S. Patent No. 6,661,100). This § 103(a) rejection should be reversed for at least the following reasons.

I. Claims 1, 7, and 8 Each Are Not Obvious over Sumikawa in view of Anderson.

The USPTO has the burden under 35 U.S.C. § 103 of establishing a *prima facie* case of obviousness. *In re Piasecki*, 745, F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). In order for a claim to be rendered obvious under § 103(a), each and every limitation of that claim must be taught or suggested in one or more references, and such teachings and suggestions must be combinable. Hindsight is not permissible. Sumikawa and Anderson, alone and in combination, fail to teach or suggest each and every limitation of claim 1 and its dependents. Thus, Sumikawa and Anderson, alone and in combination, fail to render obvious claim 1 and its dependents.

Claim 1 requires "at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply, at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground . . . at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip." In other words, at least one of the through electrodes "electrically link[s]" the front

surface of the chip to the back surface of the chip and is a "*non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip.*" For example and without limitation, see the right-hand non-contact through electrode 19 in Fig. 3 of the instant application, which is electrically isolated from the chip, and the non-contact through electrodes 19 in Figs. 8-9, along with the example description at page 17, lines 11-12, of the instant specification. The cited art, alone and in combination, fails to teach or suggest the aforesaid underlined and quoted feature of claim 1 and its dependents.

More particularly, Sumikawa and Anderson, alone and in combination, fail to teach or suggest a non-contact through electrode electrically linking the front surface of the chip to the back surface of the chip that is a "*non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip,*" as required by claim 1 and its dependents. The Examiner relies on col. 4, lines 3-6 and 45-55 of Sumikawa as allegedly disclosing for this feature. However, this portion of Sumikawa does not teach or suggest such a non-contact through electrode. This portion of Sumikawa simply states:

> "In FIG. 3, reference numeral 6 denotes an insulating film for breaking the connection of the semiconductor chip 1 with the penetrating electrode 2, the bump electrode 3, the pad electrode 4 and the wiring patterns 5a and 5b. Reference numeral 7 denotes a protective film for the semiconductor chip 1."

Clearly, then, this portion of Sumikawa alone does not teach or suggest a "non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip."

Page 9 of the Final Office Action argues that Fig. 4 of Sumikawa "shows both electrodes (2a, 22) [sic -- (2a, 22a)] in contact with pads (4a, 3a, 23a) and electrodes (2b, 22b) not in contact with any pads." It is noted that Fig. 4 of Sumikawa is only a single cross-sectional view of the first embodiment disclosed therein. However, Fig. 5 of Sumikawa shows another cross-sectional view of this same embodiment. It is clear from this figure that all penetrating electrodes (2a, 2b, 22a, 22b) are indeed in electrical contact with pads -- thus, they are not "*electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip.*"

Even if these figures are considered conflicting, there is "no legal basis for holding that one possible interpretation of ambiguous drawings shall prevail over language of a specification which conflicts with that interpretation." *See Johnson and Moore v. Riener*, 302 F.2d 757, 133 USPQ 545 (CCPA 1962). In other words, to the extent that Figs. 4 and 5 of Sumikawa are conflicting, the specification should be taken as resolving any lingering doubt as to what the drawings actually show. To this end, the specification of Sumikawa explains Figs. 4 and 5 and makes very clear that the penetrating electrodes (22a, 22b, 2a, 2b) are electrically connected to wiring patterns of the chip and transmit signals. For example, col. 4, line 60 to col. 5, line 6 of Sumikawa states that:

> "The signal input to the pad electrode 4a is transmitted to the penetrating electrode 22a of the upper semiconductor chip 21 through the wiring pattern 5a , the penetrating electrode 2a, the wiring pattern 5b, the bump electrode 3a, the pad electrode 24a and the wiring pattern 25a. . . .
>
> On the other hand, the signal input to the pad electrode 4b is transmitted to a bump electrode 23a of the upper semiconductor chip 21 through a wiring pattern 5c, a penetrating electrode 2b, a wiring pattern 5d, the bump electrode 3b, the pad electrode 24b, a wiring pattern 25c, a penetrating electrode 22b and a wiring pattern 25d, and then further transmitted to a semiconductor chip stacked thereon (not shown)."

Sumikawa thus actually teaches away from the non-contact requirement of claim 1. Sumikawa's penetrating electrodes 2a, 2b, 22a, and 22b are electrically connected to electrode pads 7 of the chip and are also connected to wiring patterns 5a. Thus, Sumikawa actually teaches an arrangement quite different from what claim 1 of the instant application requires. In particular, as noted above, claim 1 requires that a through electrode is a non-contact through electrode which is *electrically isolated from the chip so that it is not electrically connected to any electrode pad.* Because electrode 22b is part of an active circuit, as explained by Sumikawa, it cannot meet this requirement of claim 1. Accordingly, Sumikawa and Anderson, alone and in combination, fail to teach or suggest at least this feature of claim 1. Accordingly, Sumikawa and Anderson, alone and in combination, fail to render obvious the invention of claim 1 and its dependents.

Similar to claim 1, claim 7 requires that "at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed so that said least one through electrode is not electrically connected to any electrode pad of the chip," and claim 8 requires that "at least one of the through electrodes is a non-contact through electrode which is not electrically connected to any electrode pad of the chip in which it is formed." As explained above, the cited art, alone and in combination, fails to teach or suggest at least these features of each of claims 7 and 8, respectively. Accordingly, Sumikawa and Anderson, alone and in combination, fail to render obvious the invention of each of claims 7 and 8, and their respective dependents.

As such, Applicant respectfully requests that the rejection of claims 1-2, 4-5, 7-9, 11-13, 15-17, and 19-20 under 35 U.S.C. § 103(a) be reversed.

II. Claims 9, 11-13, 15-17, and 19-20 Each Are Not Obvious over Sumikawa in view of Anderson.

In rejecting claims 9, 11-13, 15-17, and 19-20, the Final Office Action asserts that it is well known that a larger total cross-section is used for a longer conduction path to reduce impedance, and further asserts that one of ordinary skill in the art at the time of the invention would connect through electrodes in order to reduce impedance. As shown below, this latter assertion certainly is based on impermissible hindsight reasoning. Accordingly, the rejection of these claims is improper.

This Board recently held that a person of ordinary skill in the art having common sense at the time of an invention would not reasonably look to a second reference to solve a problem already solved by a first reference. *See Ex Parte Rinkevich et al.*, Appeal No. 20071317, decided May 29, 2007. Similar reasoning applies here. That is, Anderson teaches reducing impedance by using a wide, thick wire at col. 3, lines 57-64. Assuming, *arguendo*, that Anderson with Sumikawa were combinable, one of ordinary skill in the art at the time of the invention wishing to reduce impedance would apply the teaching of Anderson by providing wider, thicker metal plugs in making such a combination. At first blush, it seems reasonable enough to assume that one ordinary skilled in the art looking at a reference actually would apply the teachings provided in that reference. Following this logic in connection with the alleged combination of Sumikawa and Anderson, one of

ordinary skill in the art at the time of the invention would have reduced impedance by providing wider, thicker metal plugs.

However, the pending claims call for through electrodes with substantially equal cross-sectional area. Accordingly, the incorporation of wider, thicker metal plugs into Sumikawa certainly would not render obvious claims 9, 11-13, 15-17, and 19-20. Even if one of ordinary skill in the art at the time of the invention were to combine Sumikawa and Anderson, the ordinarily skilled artisan would not have deviated from the explicit teachings of Anderson in trying to solve the problem of increasing impedance, since Anderson already explicitly solves this problem by providing wider, thicker metal plugs.

Anderson does teach connecting a plurality of solder bumps in order to provide GND and VDD to various parts of the chips. However, the connection of multiple solder bumps in Anderson is entirely unrelated to reducing impedance. Instead, impedance is reduced in Anderson by using wide, thick wires. Thus, the rationale alleged by the Examiner for the combination lacks merit and is fundamentally flawed. Differently stated, one of ordinary skill in the art would not have made the modification alleged by the Examiner to reduce impedance as alleged by the Final Office Action; instead, one would have reduced impedance by using wide, thick wires, per the actual teachings of Anderson, which would not result in the claimed inventions recited in these claims.

For at least these additional reasons, Applicant respectfully requests that the rejection of claims 9, 11-13, 15-17, and 19-20 be reversed.

CONCLUSION

In conclusion it is believed that the application is in clear condition for allowance; therefore, early reversal of the Final Rejection and passage of the subject application to issue are earnestly solicited.

Respectfully submitted,

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(VIII) CLAIMS APPENDIX

1. A semiconductor device, comprising:

a plurality of spaced apart through electrodes with equal cross-sectional areas in a semiconductor chip, which through electrodes electrically link a front surface of the chip to a back surface of the chip, wherein

at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply,

at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground,

a particular signal-routing through electrode is formed of only one of the plurality of through electrodes; and

at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip.

2. The semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip.

4. The semiconductor device as set forth in claim 1, wherein both of the first number and the second number is two or greater, so that each of the first and second

high-current through electrodes is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode is made up of only one of the through electrodes.

5. A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including a semiconductor device according to claim 1.

7. A chip-stack semiconductor device, comprising:

a plurality of stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof,

wherein at least one of a first high-current through electrode connected to a power supply and a second high-current through electrode connected to ground is made up of at least two of the through electrodes which are electrically connected to one another, whereas a signal-routing electrode connecting a front a back surface of one of the semiconductor chips is made up of only one of the through electrodes, and

at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed so that said least one through electrode is not electrically connected to any electrode pad of the chip.

8. A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof, the number of the through electrodes being determined in accordance with a magnitude of an electric current to be conducted therethrough,

wherein

adjacent connected ones of the through electrodes which are connected to a either a ground terminal or a power supply terminal of that semiconductor chip are greater in number than adjacent connected ones of the through electrodes which are connected to a particular signal terminal thereof, and

at least one of the through electrodes is a non-contact through electrode which is not electrically connected to any electrode pad of the chip in which it is formed.

9. The chip-stack semiconductor device as set forth in claim 5, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

11. The chip-stack semiconductor device as set forth in claim 7, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

12. The chip-stack semiconductor device as set forth in claim 8, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

13. The chip-stack semiconductor device as set forth in claim 5, wherein as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for the first high-current through electrode and the second high-current through electrode.

15. The chip-stack semiconductor device as set forth in claim 7, wherein the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for the first high-current through electrode and the second high-current through electrode.

16. The chip-stack semiconductor device as set forth in claim 8, wherein as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for a first high-current through electrode and a second high-current through electrode.

17. The chip-stack semiconductor device as set forth in claim 13, wherein numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

19. The chip-stack semiconductor device as set forth in claim 15, wherein numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

20. The chip-stack semiconductor device as set forth in claim 16, wherein numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

(IX) EVIDENCE APPENDIX

None.

(X) RELATED PROCEEDINGS APPENDIX

None.